IN THE DRAWINGS

The attached sheets of drawings include changes to Figures 1 and 2. These sheets replace the original sheets, including Figures 1 and 2.

REMARKS

Reconsideration of this application, as amended, is respectfully requested. Claims 1-29 are pending in the application. Claims 1, 2, 9, 25, and 27 have been amended. No claims have been added. Claims 5 and 26 have been canceled without prejudice.

Applicants have amended the claims to more clearly point out what Applicants regard as their invention. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. No new matter has been added.

Revisions to the Specification and Drawings

The Examiner objected to Figure 1 in the Office Action. Applicants propose to amend Figure 1 by replacing "PROCESSOR(S) 102-104" with "PROCESSOR(S) 102, 104". A red-lined copy of Figure 1 is enclosed for the Examiner to review. A clean copy of amended Figure 1 and another red-lined copy will be forwarded to the Chief Draftperson. Applicants respectfully request the Examiner to approve the proposed amendment to Figure 1 and to withdraw the objection.

The Examiner objected to the drawing because the multiple references to "functional units 212-218" do not coincide with the drawing in Figure 2. Applicants propose to amend Figure 2 by removing the ellipsis between FUNCTIONAL UNIT 216 and FUNCTIONAL UNIT 218 and placing a new set of ellipsis below FUNCTIONAL UNIT 218. Furthermore, the applicants have amended the specification to refer to "functional units 212, 214, 216, and 218" instead of "functional units 212-218" so that references to Figure 2 in the specification correspond with the drawing in Figure 2. Applicants respectfully submit that no new matter has been added. Applicants respectfully request the Examiner to approve the proposed amendment to Figure 2 together with the amendments to the specification and to withdraw the objection.

The Examiner objected to Figure 3 because it contained a "reference sign(s) not mentioned in the description: "314" in Fig. 3" (Office Action, page 2, paragraph 4). The applicants respectfully submit that process block 314 was disclosed in paragraph 0060 of the application as originally filed. Therefore, Applicants request the Examiner to withdraw the objection.

Rejections Under 35 U.S.C. §112, Second Paragraph

Claim 27 stands rejected under 35 U.S.C. §112 as lacking sufficient antecedent basis for limitations within the claims. Applicants respectfully traverse the rejection.

Applicants respectfully submit that claim 27, as amended, satisfies the requirements of 35 U.S.C. §112, second paragraph, and respectfully requests the withdrawal of the rejection of the claims under §112.

Rejections Under 35 U.S.C. §102(b)

Claims 1, 7-9, 11, 12, 25, 28, and 29 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,802,373, of Yates, et al. (hereinafter "Yates"). Applicants respectfully traverse the rejection.

The Examiner argued in the office action that:

> *Yates et al.* discloses receiving a binary of a program code, the binary based on a first instruction set architecture (see, for example, the Abstract); and translating the binary, wherein the translated binary is based on a combination of the first instruction set architecture and a second instruction set architecture (see for example, the Abstract).

(Office Action, page 4, paragraph 2).

The Applicants respectfully disagree with the Examiner and submit that Yates does not anticipate the Applicants' invention because Yates fails to disclose each and every element of the invention as claimed.

Claim 1, as amended, teaches:

> [R]eceiving a binary of a program code, the binary based on a first instruction set architecture; [¶] translating the binary, wherein the translated binary is based on a combination of the first instruction set architecture and a second instruction set architecture; and [¶] executing the translated binary according to the second instruction set architecture.

Applicants respectfully submit that Yates does not disclose translating and executing a binary "wherein the translated binary is based on a combination of the first instruction set architecture and a second instruction set architecture." Furthermore, Yates does not disclose "executing the translated binary according to the second instruction set architecture."

In contrast, Yates discloses a system where a binary is executed in two environments, either as a translated image within the native environment or an interpreted image of the non-native image (Yates, Abstract). Yates describes translating functions when requested by a user. If a function is requested for the first time, it is entirely translated to equivalent native code (Yates, column 11, lines 39-52). But, if the code was previously translated according to a user request, Yates merely loads the image of the fully translated code from memory (Yates, column 8, line 53 to column 9, line 20). However, since Yates completely translates a binary when requested by a user, any binary that is executed according to Yates is based entirely on the native ISA and not a "combination of the first instruction set architecture and a second instruction set architecture" as claimed by the Applicants in claim 1. Therefore, Yates does anticipate claim 1.

Accordingly, Applicant respectfully submits that the invention claimed in claim 1 is not anticipated by Yates under 35 U.S.C. §102(b) for at least the reasons discussed above and respectfully requests the withdrawal of the rejection.

Claims 7 and 8 depend, indirectly on claim 1. Since Yates does no anticipate claim 1 as discussed above, Yates does not anticipate claims 7 and 8 for at least the same reasons. Applicants respectfully request withdrawal of the rejections.

Claim 9 as amended contains language similar to that used in claim 1. For at least the reasons discussed above with respect to claim 1, Yates does not anticipate claim 9. Applicants respectfully request withdrawal of the rejection.

Claims 11 and 12 depend, directly or indirectly on claim 9. Since Yates does not anticipate claim 9 as discussed above, Yates does not anticipate claims 11 and 12 for at least the same reasons. Applicants respectfully request withdrawal of the rejections.

Claim 14 as amended and claim 17 are system versions of the claimed methods of claims 9 and 12, respectively. Since Yates does not anticipate claims 9 and 12 as discussed above, Yates does not anticipate claims 14 and 17 for at least the same reasons. Applicants respectfully request withdrawal of the rejections.

Claim 25, 28, and 29 are machine-readable medium versions of the claimed methods in claims 1, 7, and 11, respectively. Since Yates does not anticipate claims 1, 7, and 11 as discussed above, Yates does not anticipate claims 25, 28, and 29 for at least the same reasons. Applicants respectfully request withdrawal of the rejections.

Rejections Under 35 U.S.C. §103(a)

Claim 10 was rejected under 35 U.S.C. §103(a) as being obvious over Yates in view of Bich C. Le, "An Out-of-Order Execution Technique for Runtime Binary Translators," 1998 (hereinafter Le). The Applicants respectfully traverse the rejection for at least the same reasons discussed above with respect to claim 1.

Furthermore, Applicant respectfully submits that neither Yates nor Le, alone or in combination, disclose each and every element of the invention as claimed. Le discloses a system which, when executed, converts a binary from a first ISA that has in-order access to memory to a second ISA that has out-of-order access to memory. Le facilitates the translation to out-of-order memory using instruction emulation and "checkpoints" within the translation in order to handle exceptions (Le, section 1.2). Similarly to Yates as discussed above with respect to independent claim 9, Le discloses a system that does automatic translation; in particular, Le describes a system that makes exception handling between two ISAs transparent (Le, section 1.1 and 1.2). However, as discussed above, the Applicants' invention provides that "the translated binary [is] based on a combination of the first instruction set architecture and the second instruction set architecture," as claimed in amended claim 9. Because Le fails to disclose a translated binary based on a combination of the first and second ISA, neither Yates nor Le, alone or in combination, disclose each and every limitation as claimed by the inventors in claim 10, with respect to independent claim 9.

Furthermore, there is no suggestion or motivation within Yates or Le to combine the references in such a way as to render claim 10 obvious. Yates discloses a method and system of automatically translating a non-native binary when the binary is executed on a native system. Le, on the other hand, discloses a system and method for handling exceptions in user programs. However, Le states that "[t]he design does not rely on native OS services to process exceptions, therefore it only supports the emulation of user level programs, not system code" (Le, section 1.2). Therefore, the disclosure of Le is limited to user level programs and does not function with the translation of system level code. Because Le admits that the disclosure is limited to a specific kind of computer code, one of ordinary skill in the art would not be motivated to combine Yates and Le to solve the problem of creating a general binary translator, as taught in claim 10, with respect to independent claim 9.

Therefore, the combination of Yates and Le cannot render obvious Applicants' invention as claimed in claim 10. Applicants respectfully request the withdrawal of the rejection of the claims under 35 U.S.C. §103(a) over the combination, for at least the reasons discussed above.

Claims 2-6, 13, 15, 16, 18-24, 26, and 27 were rejected under 35 U.S.C. §103(a) as being obvious over Yates in view of U.S. Patent No. 6,496,922, of Borrill (hereinafter "Borrill"). Applicants respectfully traverse the rejections for the reasons discussed above with respect to claim 1 and, at least, the following reasons.

Claim 2 sets forth "checking instruction set architecture execution flags, the instruction set architecture execution flags to indicate at least one translation of a portion of the binary."

The Examiner admitted that Yates does not describe the use of ISA execution flags (Office Action, page 7, paragraph 2), but argued Borrill discloses "the use of instruction set architecture execution flags (an ISA tag) indicating the native ISA for 'visiting' code" (Office Action, page 7, paragraph 2). It is respectfully submitted that Borrill does not disclose the use of ISA execution flags to indicate at least one translation of a portion of a binary. Instead, Borrill discloses the use a single identifier tag to route non-native ISA instructions to a Dynamic Decode Unit (DDU) that corresponds to the instruction's native ISA (Borrill, column 4, lines 15-29; column 5, lines 1-29). Therefore, Borrill merely discloses an identifier that acts as routing information for a non-native instruction that corresponds to a specific DDU in a system of many DDUs. The "instruction set architecture execution flags", as claimed in claim 2, do not function to route data to a specific source, but instead function to specify "at least one translation" of an instruction. Therefore, an identifier tag that routes data to the appropriate source is not the same as "instruction set architecture execution flags [that] indicate at least one translation of a portion of the binary", as claimed in claim 2.

Furthermore, Borrill discloses "simply tagging each imported block of code appropriately" such that the single tag corresponds to the code's native environment (Borrill, column 3, lines 8-9). That is, a single flag informs the system as to which architecture and DDU the code corresponds to. The applicants, however, claim multiple "instruction set architecture execution flags." The flags correspond to the translation, or translations, "based on a combination of the first instruction set architecture and the second instruction set architecture," as claimed in claim 2.

Since the combination of Yates and Borrill does not disclose each and every limitation in claim 2, the combination does not render claim 2 obvious under 35 U.S.C. §103, for at least the reasons discussed above. Applicants respectfully request the examiner to withdraw the rejection.

Claims 3-6 depend, directly or indirectly, on claim 2 and include features that further limit claim 2. Therefore, the Applicants respectfully submit that for at least the reasons advanced above with respect to claim 2, claims 3-6 are not obvious under 35 U.S.C. §103 over Yates in view of Borrill.

Furthermore, the Examiner rejected claim 13 under 35 U.S.C. §103(a) as being unpatentable over Yates in view of Borrill. Applicants respectfully traverse the rejection for the reasons discussed above with respect to independent claim 9.

Furthermore, the Applicant respectfully submits neither Yates nor Borrill, alone or in combination, disclose each and every element of the invention as claimed. Borrill discloses a system that takes a 32-bit instruction from a 32-bit ISA and appends another 32 bits to the instruction, which acts as a 64-bit instruction and DDU address (Borrill, column 7, lines 1-32). In particular, Borrill discloses a system that translates a 32-bit ISA instruction into a 64-bit very long word (VLIW) instruction (Borrill, Abstract; column 7, lines 1-32). However, as discussed above, the Applicants' invention includes translating a binary such that "the translated binary [is] based on a combination of first instruction set architecture and the second instruction set architecture." Although Borrill amends a 32-bit instruction to a VLIW instruction, the resulting instruction is based entirely on the 64-bit VLIW architecture. Therefore, neither Yates nor Borrill, alone or in combination, disclose each and every limitation as claimed by the inventors in claim 13, with respect to claim 9.

In addition, the Examiner argued that "Yates et al. fails to expressly disclose data accessed by the binary being stored in a single segment in memory and wherein an offset value for translating a virtual address to a physical address for the data is not modified during execution of the binary. However, Borrill teaches such handling of non-native addressing without modifying the non-native offset address" (Office Action, paragraph spanning pages 8-9). With respect to claims 13, 18, and 24, the Applicants respectfully submit that Yates in view of Borrill fails to teach "such handling of non-native addressing," as argued by the examiner.

Applicants respectfully submit that Yates and Borrill in combination fail to disclose each and every limitation of the Applicants invention, as claimed in claim 13 for at least the reasons

discussed above. Further, one of ordinary skill in the art would not seek to combine Yates and Borrill. Therefore, the combination of Yates and Borrill cannot render obvious Applicant's invention as claimed in claim 13, and Applicant respectfully requests the withdrawal of the rejection.

Claim 15, 16, and 18 are system versions of the claimed methods of claims 4, 3, and 13, respectively. Since Yates in view of Borrill does not render claims 4, 3, and 13 obvious under 35 U.S.C. §103(a), for at least the reasons discussed above, claims 15, 16, and 18 are nonobvious for at least the same reasons. Applicants respectfully request withdrawal of the rejections.

Claims 19-24 are apparatus versions of the claimed methods of claims 4, 7, 8, and 11-13, respectively. Since Yates in view of Borrill does not render claims 4, 7, 8, and 11-13 obvious under 35 U.S.C. §103(a), for at least the reasons discussed above, claims 19-24 are nonobvious for at least the same reasons. Applicants respectfully request withdrawal of the rejections.

Claims 26 and 27 are apparatus versions of the claimed methods of claims 5 and 6, respectively. Since Yates in View of Borrill does not render claims 5 and 6 obvious under 35 U.S.C. §103(a), for at least the reasons discussed above, claims 26 and 27 are nonobvious for at least the same reasons. Applicants respectfully request withdrawal of the rejections.

SUMMARY

Claims 1-29 are currently pending. In view of the foregoing amendments and remarks, Applicant respectfully submits that the pending claims are in condition for allowance, and such action is earnestly solicited. Applicant respectfully requests reconsideration of the application and allowance of the pending claims.

Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

Respectfully submitted,

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Ines Francetic 11/4/2004
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